REMARKS

Claims 2 – 4 and 6 – 9 remain in the application. Claims 1 – 9, 12 and 13 are rejected. Claims 2 – 4 and 6 – 9 are amended herein. Claims 1, 5, 12 and 13 are canceled herein and claims 10 and 11 are previously canceled. New claims 14 – 24 are added. No new matter has been added.

Claims 1 and 5 are canceled and rewritten as new claims 14 and 20, and claims 6 and 9 are amended to more clearly recite the invention, e.g., reflecting data flow through the recited apparatus. Claims 2 – 4, 7 and 8 are amended responsive to cancellation of claim 1 and amendment of claim 6. New claims 14 and 20 and amended claims 6 and 9, therefore, are supported by canceled claims 1 and 5 and by the specification, as filed.

Essentially, the present application is directed to "a high speed print controller [that, i]nstead of custom hardware and expensive fast multiprocessor machines, [includes a] controller [of] … cheap commodity processors such as commercial, off the shelf, personal computer systems." Page 3, lines 2 – 5. Thus, the apparatus of claim 14 is (rewritten from claim 1 and claim 20 rewritten from claim 5 are) directed to the high speed print controller (and printer including the controller) so described, made of one or more "cheap commodity processors such as commercial, off the shelf, personal computer systems," i.e., stand alone computers or personal computers.

Further, new claims 14 and 20 reflect that the controller data stream is bi directional. "By 'bi directional' what is meant is, a synchronization mechanism is provided between the host (e.g., a print server or other data stream generator) and the receiver (e.g., a printer or other output device) allowing them to synchronize at various points in the data stream." Page 5, lines 6 – 9. Also, new claims 14 and 20 recite that the "sequencer 21 is the 'main coordinator' in the controller and knows which page is at which point in the pipeline." Page 6, lines 21 – 22. Thus, "the sequencer 21 may

function as a synchronizer, issuing a command to the RIP machine to send the appropriate colorplanes of processed sheetsides as needed by the print head drivers 24a et seq." Page 8, lines 20 – 23.

As further recited by claim 20 (rewritten from claim 5), also recited in new claims 15, 16 and 21, and in amended claims 6 and 9, the controller may be one or include multiple computers, e.g., "personal computer systems." *Supra*. This is also supported throughout the specification.

> The design proposed here breaks the printer controller 10 into a pipeline with three logical stages. In the most general implementation, **each stage** is run on one or more **separate machines**. In other implementations contemplated by this invention the stages may be consolidated into a smaller number of machines or even a single machine having sufficient processing capability to perform the necessary computational steps.

Page 6, lines 12 – 18 (emphasis added).

As recited by new claims 17 – 19, 22 and 23, "the RIP machines can be of varying sizes and may be significantly different than the sequencer. For example, the sequencer 21 may be a high end machine with excellent I/O performance, while the RIP machines 22a et seq may be much cheaper and slower." Page 7, lines 21 – 24.

Claims 18, 23 and 24 are directed to communications between the sequencer and RIP machines. "The sequencer maintains a queue of the independent work units that were generated in this way. This queue is accessed by the Page RIP processors in the next pipeline stage." Page 7, lines 9 – 12. Also, "[d]epending on the size and speed of the RIP machines, each may be working on multiple work units." *Id*, lines 19 – 20. No new matter is added. Thus claims 2 – 4 and 6 – 9, as amended, and new claims 14 – 24 are all different than, and are not taught or suggested by, any reference of record, alone or further in combination with each other.

Claims 12 and 13 are objected to. Objection to the claims is obviated by cancellation of claims 12 and 13. Reconsideration and withdrawal of the objection to the claims is respectfully requested.

Claims 1 – 9, 12 and 13 are rejected under 35 USC §112. Partially responsive thereto claims 1, 5, 12 and 13 are canceled herein. Further, the recitations upon which this rejection is based is not reflected in the remaining claims, as amended, or in the new claims. Reconsideration and withdrawal of the rejection of the claims under 35 USC §112 is respectfully requested.

Claims 1, 3 and 12 are rejected under 35 USC §103(a) as being unpatentable over U.S. Patent No. 6,825,943 to Barry et al. in view of U.S. Patent No. 6,315,390 to Fujii and U.S. Patent No. 6,327,050 to Motamed. Claim 2 and 6 – 9 are rejected under 35 USC §103(a) as being unpatentable over Barry et al., Fujii and Motamed in further view of U.S. Patent No. 6,532,016 to Venkateswar et al. Claim 4, 5 and 13 are rejected under 35 USC §103(a) as being unpatentable over Barry et al., Fujii and Motamed in further view of U.S. Patent No. 5,946,460 to Hohensee et al.

Barry et al. teaches an instruction operator 114 that is connected to a "distributor block 118 [that] is provided to distribute in multiple print job files, each multiple thereof having a select portion of the print job which was segmented or partitioned by instruction operator 114 for processing according to separate processes in a plurality of parallel sections of the print system illustrated in FIGS. 1a and 1b." Col. 5, lines 8 – 14. So, the output of the Barry et al. instruction operator 114 is connected to a single Barry et al. functional unit, i.e., distributor 118. The Barry et al. "distributor 118 provides the print job file 104 including a first select portion 140 along a line 142 to a first RIP engine 150." *Id*, lines 14 – 16. The Barry et al, figures show data and signals flowing in one direction, in to out. Therefore, because Barry et al. requires this intervening distributor 118 and because Barry et al. shows data and signals flowing only in one direction, the

Barry et al. instruction operator 114 is not communicating bi-directionally with the RIP engines and certainly not with the print drivers. Neither is the Barry et al. instruction operator 114 the main controller synchronizing print jobs in the controller pipeline.

Fujii et al. Figure 3 is a block diagram showing the control circuit 30 of a printer. The control circuit 30 includes a line inkjet head 35 with a head driver 34 driving an ink jet head 5. It is apparent that the Fujii et al. head driver 34 is not a processor or computer, but has application to a low cost commodity printer connected to a personal computer 32. Therefore, the Fujii et al. head driver 34 is not one or more print driver processors or one or more print driver computers as the new and amended claims recite. Nor does Fujii et al. teach or suggest replacing head driver 34 with one or more print driver processors or one or more print driver computers 32 as the new and amended recite.

While Motamed teaches a "multiple raster image processor (RIP) system which enables faster system performance over multiple processors" (Abstract), Motamed figures show data and signals flowing (arrowheads) in one direction. The Motamed "scheduler sends the original print instruction file **to all of the processors**, as well as a list 38 of which pages are assigned to which processor." Col. 4, lines 47 – 49 (emphasis added). Clearly this describes a "fire and forget" operation, not a networked operation with a sequencer maintaining overall control. As is apparent from Motamed Figure 6, the RIP processors 66, 67, communicate with a video print machine 24 "(It maintains a list of job/page numbers already processed by all the RIPS)," not with print engine processors after 75. Col. 6, lines 32 – 32. "The RIPs are connected to one or more video print machines 64 via a high speed interconnect bus 74. The video print machine provides output to a print engine 75" from cached print data 65. Col. 26 – 30. Clearly, communication with the print engine 75 is not bi-directional and certainly not with the Motamed scheduler 62.

Therefore, the combination of Barry et al., Fujii and Motamed fails to result in the present invention, as recited in claim 14 or any claims 15 – 19 and 3 depending therefrom. Reconsideration and withdrawal of the rejection of claim 3 (and 14) under 35 USC §103(a) is respectfully requested.

In rejecting claims 4 and 5 (now 20), Hohensee et al. is relied on to "disclose each of said raster image processors converts data from a form communicated as a print data stream into a variable number of portions depending upon whether an individual page is to be blank or to be printed with a single color or to be printed with multiple colors (col. 4, lines 53-60)." Page 10. Regardless of whether that is what Hohensee et al. discloses, for the reasons set forth above with respect to claim 14, the addition of Hohensee et al. to Barry et al., Fujii and Motamed fails to result in the present invention, as recited in claim 4, 20 or any of claims 21 – 24 depending therefrom. Reconsideration and withdrawal of the rejection of claims 4 and 5 (now 20) under 35 USC §103(a) is respectfully requested.

In rejecting claims 2 and 6 – 9, Venkateswar et al. is relied on to "disclose queuing packaged print stream data portions and communicating packaged print stream data portions directly to a plurality of raster image processors (col. 2, lines 21-28)." Page 12. Actually, Venkateswar et al. describes the RIP processors participating in packaging and queuing. Venkateswar et al. teaches a "main processor (52) of a **single-chip multiprocessor** converts an incoming page of print data into paths. The paths are then converted to primitives and the primitives are rasterized using parallel processor (60, 62, 64, 66). The parallel processors (60, 62, 64, 66) work in concert with the main processor (52) … ." Abstract (emphasis added). So, "the main processor creates the paths using some assistance from the parallel processors to accelerate the tasks. This is typically done by using a task queue, **with all of the parallel processors** eligible to assist. The parallel processors then perform the boundary processing part of geometry processing," using, presumably, shared resources, e.g., memory. Col. 2, lines 21 – 27 (emphasis added).

Clearly, Venkateswar et al. alone or in combination with Barry et al., Fujii and Motamed, fails to describe or suggest, a computer queuing work units for RIP PCs, as claims 6 and 9 are amended to recite. Therefore, and for the reasons set forth above with respect to claims 14 and 20, the addition of Venkateswar et al. to Barry et al., Fujii and Motamed fails to result in the present invention, as recited in claims 2, 6 or 9 or any claims depending therefrom. Reconsideration and withdrawal of the rejection of claims 2 and 6 – 9 under 35 USC §103(a) is respectfully requested.

The applicants thank the Examiner for efforts, both past and present, in examining the application. Believing the application to be in condition for allowance, both for the amendment to the claims and for the reasons set forth above, the applicants respectfully request that the Examiner consider new claims 14 – 24, reconsider and withdraw the objection to the claims, reconsider and withdraw the rejection of claims 2 – 4 and 6 – 9 under 35 U.S.C. §§103(a) and 112, and allow the application to issue.

As previously noted MPEP §706 "Rejection of Claims," subsection III, "PATENTABLE SUBJECT MATTER DISCLOSED BUT NOT CLAIMED" provides in pertinent part that

> If **the examiner** is satisfied after the search has been completed that patentable subject matter has been disclosed and the record indicates that the applicant intends to claim such subject matter, he or she **may note** in the Office action that **certain aspects or features** of the patentable invention have not been claimed and that if properly claimed such claims **may be given favorable consideration**. (emphasis added.)

The applicants continue to believe that the written description of the present application is quite different than, and not suggested by, any reference of record. Accordingly, should the Examiner believe anything further may be required, the Examiner is requested to contact the undersigned attorney at the local telephone number listed below for a telephonic or personal interview to discuss any other changes.

Please charge any deficiencies in fees and credit any overpayment of fees to IBM Corporation Deposit Account No. 50-3669 and advise us accordingly.

Respectfully Submitted,

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(Date)

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